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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,611	09/09/2003	Qi Xiang	039153-0685	2532

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,611	XIANG, QI	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 5/11/05. Currently, claims 1-4 and 6-20 are pending.

Drawings

Objection to the drawings under 37 CFR 1.83(a) has been maintained for reasons of record. The drawings must show every feature of the invention specified in the claims. Therefore, **the point defects in layer 20 must be shown** or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-8, 10, and 12-20 under 35 U.S.C. 103(a) as being unpatentable over Nakaoka et al., US Patent 6,337,500 in view of Baba US Patent 6,852,604.

Nakaoka discloses the semiconductor method substantially as claimed. See figures 1-14, and corresponding text, where Nakaoka shows, pertaining to claim 1, a method for forming a semiconductor device, comprising: providing a substrate **301** having formed therein a layer of silicon **303**; implanting a species to create point defects **315** (lattice defect) in the silicon layer at a source region of an NMOS device to extend the duration of a transient region of n-type dopant diffusivity in the silicon of the source region (figure 4b; col. 4, lines 35-60, which also shows types of ions used to form point defects; col. 11, lines 10-15, the Examiner takes the position that since ~~the~~ Nakaoka teaches an implantation of the exact same species materials as the Applicant's disclosure, an extended duration transient region of n-type dopant diffusivity will occur);

S.T.

implanting n-type dopant into the silicon layer to form source **309** and drain **310** regions of the NMOS device (figure 4d; col. 11, lines 35-43); and annealing to activate the n-type dopant in the source and drain regions of the NMOS device, wherein said point defects retard n-type dopant diffusion during said activation (figure 4d; col. 11, lines 35-43, ***Note***: Since Nakaoka shows the formation of point defects prior to the formation of the source and drain regions, the retardation of the n-type dopants would be performed, since Nakaoka teaches the same steps as Applicant's disclosure). In addition, Nakaoka shows, pertaining to claim 2, the method, wherein creating said point defects is performed prior to implanting shallow source and drain extensions of the NMOS device (figure 7e; col. 13, lines 45-57). In addition, Nakaoka shows, pertaining to claim 6, the method, wherein creating said point defects is performed subsequent to implanting deep source and drain regions of the NMOS device (figure 7; col. 14, lines 55-67). Also, Nakaoka shows, pertaining to claim 7, the method wherein creating said point defects is performed prior to implanting said n-type dopant (figure 4 and 6; col. 14, lines 55-67). Nakaoka shows, pertaining to claim 8, wherein creating said point defects is performed after implanting said n-type dopant (figure 7; col. 13, lines 45-56). Also, Nakaoka shows, pertaining to claim 10, the method, wherein said species is also implanted into the silicon layer in a drain region of the NMOS device to extend the duration of transient region of n-type dopant diffusivity in the silicon of the drain region (figure 7e; col. 13, lines 46-57). In addition, Nakaoka shows, pertaining to claim 12, the method wherein the species implanted to create point defects is germanium (col. 14, lines 29-39). Also, Nakaoka shows, pertaining to claim 13, the method wherein the species implanted to create defects in silicon (col. 14, lines 29-39). Nakaoka shows, pertaining to claim 14, the method, wherein the species implanted to create point defects is an

inert element (col. 14, lines 29-39). Also, Nakaoka shows, pertaining to claim 15, the method wherein the silicon layer is formed on a silicon substrate (figure 7a; col. 13, lines 1-10). In addition, Nakaoka shows, pertaining to claim 16, the method wherein the silicon layer is formed on a dielectric layer (figure 7a; col. 12, lines 65-67). In addition, Nakaoka shows, pertaining to claim 19, the method, wherein the NMOS device includes the silicon layer in a channel region **314** (figure 7c; col. 13, lines 15-18). Finally, Nakaoka shows, pertaining to claim 20, the method of forming an NMOS device, comprising: forming a structure comprising n-type source and drain regions implanted in a silicon layer of a substrate, wherein the silicon of at least the source region contains point defects created by implantation of a species other than an n-type dopant (col. 13, lines 19-56); and annealing to activate the source and drain regions, wherein said point defects retard n-type dopant diffusion during said activation (col. 13, lines 19-56; col. 14, lines 40-67).

However, Nakaoka fails to show, pertaining to claims 1-20, providing a substrate comprising a layer of silicon germanium having formed thereon a layer of strained silicon. In addition, Nakaoka fails to show, pertaining to claim 3, the method, wherein creating said point defects is performed subsequent to implanting shallow source and drain extensions of the NMOS device and prior to forming a spacer around a gate of the NMOS device. Also, Nakaoka fails to show, pertaining to claim 4, the method, wherein creating said point defects is performed subsequent to forming a spacer around a gate of the NMOS device and prior to implanting deep source and drain regions of the NMOS device. Nakaoka fails to show, pertaining to claim 17, the method, wherein said annealing is performed for a time that is less than the duration of the transient region of n-type dopant diffusivity in the silicon germanium of the source region having

said point defects created therein. Finally, Nakaoka fails to show, pertaining to claim 18, the method, wherein said annealing comprises performing multiple anneals, each said multiple anneals being performed for a time that is less than the duration of the transient region of n-type dopant diffusivity in the silicon germanium of the source region having said point defects created therein.

Baba teaches, in figures 1(a)-3(e), and corresponding text, a similar method for forming a semiconductor device, pertaining to claims 1-20, where a silicon germanium layer is formed on a silicon substrate and a strained silicon layer is formed over the silicon germanium layer. In addition, Baba teaches the advantages of using a hetero structure device (col. 5, lines 45-62).

It would have been obvious to one of ordinary skill in the art to, substitute, providing a substrate comprising a layer of silicon germanium and having formed thereon a layer of strained silicon, in the method of Nakaoka, pertaining to claims 1-20, according to the teachings of Baba, with the motivation that creating a hetero structure device using the silicon germanium substrate and, forming a strained silicon layer thereon, as taught by Baba, having a lattice constant that is different from silicon, achieves an increase in the speed of a MOSFET device, resulting in a more efficient semiconductor device.

It would have been obvious to one of ordinary skill in the art to incorporate, the method, wherein said annealing is performed for a time that is less than the duration of the transient region of n-type dopant diffusivity in the silicon germanium of the source region having said point defects in Applicant's disclosure, created therein; the method, wherein said annealing comprises performing multiple anneals, each said multiple anneals being performed for a time that is less than the duration of the transient region of n-type dopant diffusivity in the silicon

germanium of the source region having said point defects created therein, in the method of Nakaoka, pertaining to claims 17 and 18, according to both the teachings of Nakaoka and Baba, with the motivation that, the point defects (lattice defects) taught by Nakaoka and Baba, includes the same elements used to form the point defects, and are implanted prior to the activation of the dopants, resulting in an overall lower dopant diffusivity during activation. Therefore, the annealing or multiple annealing being performed would prove to be less, since there would be less duration time needed to perform the diffusion of the dopant materials.

It would have been obvious to one of ordinary skill in the art to incorporate the following steps of: wherein creating said point defects is performed subsequent to implanting shallow source and drain extensions of the NMOS device and prior to forming a spacer around a gate of the NMOS device; wherein creating said point defects is performed subsequent to forming a spacer around a gate of the NMOS device and prior to implanting deep source and drain regions of the NMOS device, in the method of Nakaoka, pertaining to claims 3 and 4, according to the combined teachings of Nakaoka and Baba, with the motivation that, both Nakaoka and Baba, teach the formation of conventional NMOS devices, where Nakaoka shows the formation of a point defects within the NMOS semiconductor layer. Therefore, whether creating the point defects prior to forming a spacer around a gate, or subsequent to forming the spacer and prior to implanting deep source and drain regions, would prove to be equivalent, since the ultimate goal is to form point defects within the semiconductor layer of the NMOS device.

Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaoka et al., US Patent 6,337,500 in view of Baba US Patent 6,852,604 in view of Yamamoto US Patent 6,710,407.

Nakaoka in view of Baba discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1-4, 6-8, 10, and 12-20 under 35 U.S.C. 103(a).

However, Nakaoka fails to show, pertaining to claim 9, the method, wherein creating said point defects comprises selectively masking the substrate to protect an active region of a PMOS device on the substrate and to protect a drain region of the NMOS device. In addition, Nakaoka fails to show, pertaining to claim 11, the method, wherein creating said point defects comprises selectively masking the substrate to protect an active region of PMOS device on the substrate.

Yamamoto teaches, in figures 2A-9, and corresponding text, a conventional CMOS device that includes protecting the active regions of both a NMOS and a PMOS device during an ion implantation technique (col. 6, lines 17-45; col. 8, lines 16-63).

It would have been obvious to one of ordinary skill in the art to incorporate the following steps of: wherein creating said point defects comprises selectively masking the substrate to protect an active region of a PMOS device on the substrate and to protect a drain region of the NMOS device; wherein creating said point defects comprises selectively masking the substrate to protect an active region of PMOS device on the substrate, in the method of Nakaoka in view of Baba, pertaining to claim 9 and 11, according to the teachings of Yamamoto, with the motivation, that since CMOS devices conventionally include both NMOS and PMOS devices having different active regions, utilizing a mask to cover the PMOS device or visa versa, would

be routine in controlling the ion implantation of impurities within specific regions of both the NMOS and PMOS devices.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY PATENT EXAMINER
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Stanetta Isaac
Patent Examiner
July 18, 2005